UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,507	03/10/2004	Steven E. Boor	30521/3070A	3966

4743 7590 07/23/2008

MARSHALL, GERSTEIN & BORUN LLP
233 S. WACKER DRIVE, SUITE 6300
SEARS TOWER
CHICAGO, IL 60606

EXAMINER	
OLANIRAN, FATIMAT O	
ART UNIT	PAPER NUMBER
2615	

MAIL DATE	DELIVERY MODE
07/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,507	BOOR, STEVEN E.	
	Examiner	Art Unit	
	FATIMAT O. OLANIRAN	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/17/2008 have been fully considered but they are not persuasive

Applicant argues with regard to claim 1, "Levitt et al. fail to teach or suggest a buffer circuit for a microphone assembly."

Examiner respectfully disagrees; Levitt discloses programmable amplifier, (Fig. 2 element 58) and programmable filters (Fig. 2 element 64). One of ordinary skill in the art at the time the invention was made would infer that amplifier 58 acts as a preamplifier or buffer circuit by raising the microphone output to the necessary level for the remaining signal processing. In addition a buffer is simply an amplifier used to isolate the preceding input circuitry from the load output.

Applicant argues, "…Levitt et al. do not describe adjusting a characteristic of the filter network using a first input nor a tuning circuit responsive to the selector…"

Examiner respectfully disagrees; Levitt discloses a programmable filter, (col. 5 line 3-4, element 64) and a tuning circuit (EEPROM col. 5 line 36-37) and a selector circuit (host controller col. 5 line 36-37). In order to overcome a prior art rejection applicant must specifically point out how applicant's claims differ over the prior art. Simply asserting a difference does not overcome the prior art.

With regards to claim 15, applicant argues, "... Levitt et al. do not describe whether the substrate is separable into at least first and second portions such that the buffer circuit disposed on the first portion is separable from the second portion of the substrate."

Examiner respectfully disagrees; a substrate is inherent to a circuit because a substrate is simply the base material or platform for a circuit implementation. Levitt et al discloses two circuits (Fig. 1 and Fig. 2) and therefore first and second portion substrates.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1-3, 9-10, 12-17, 19-20 and 22 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Levitt et al. (4879749).

Claim 1 Levitt discloses a buffer circuit (Fig. 1-2, host controller, EEPROM, filter and amplifier) for use in a microphone assembly comprising:

A microphone housing (Fig. 2 and col. 3 line 39-41)

an input for receiving a signal (Fig. 2: microphone 57); an input buffer (Fig. 2; element 58 PROGR AGC) coupled to the input; an output (col. 5 line 7-11); a filter network coupled (Fig. 2: element 64) between the input buffer and the output; a selector (Fig. 1;host controller col. 3 line 36, Fig. 2; 84: EEPROM) comprising: a first input (col. 4 line

30-33 output host controller); a first output responsive to the first input (col. 2 line 49-51output EEPROM); and a tuning circuit (Fig. 2; 84 :EEPROM, tri-state switches, 85-86) coupled to the filter network for adjusting a characteristic of the filter network (col. 2 line 49-51), the tuning circuit responsive to the selector (col. 5 line 36-37),and the characteristic of the filter network is adjusted using the first input (col. 5 line 36-37) Levitt does not disclose wherein the buffer circuit is contained in the microphone housing (Fig. 2 and col. 3 line 39-41)
However Levitt discloses wherein elements of the buffer circuit are contained in the microphone housing (Fig. 2 and col. 3 line 39-41).
Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made that the placement of selected elements within a housing would be determined by space considerations and design choice.

Claim 2 Levitt discloses, wherein the first input is on a separable tab (Fig. 1:124, EEPROM programming socket, col. 8 line 25-29).

Claim 3 analyzed with respect to claim 1, Levitt discloses, wherein the first input is on a separable tab (Fig. 1:124, EEPROM programming socket) and the characteristic of the filter network (col. 5 line 38-40) is adjusted (col. 8 line 25-29). Levitt does not clearly disclose wherein the first input is on a separable tab and the separable tab is removed from the buffer circuit after the characteristic of the filter network is adjusted. However it

would be obvious to one ordinarily skilled in the art at the time the invention was made to place the host controller on a separable tab so that the buffer circuit can be removed from the programming device after programming and so user will not have to use the microphone assembly with an additional circuit or device attached.

Claim 9, Levitt discloses, wherein the first input is coupled to a biasing element (col. 5 line 34-37).

Claim 10, Levitt discloses, wherein the biasing element maintains a persistent state responsive to a programming signal applied to the first input (col. 5 line 34-37).

Claim 12, Levitt discloses wherein the biasing element is an EEPROM (col. 5 line 34-37).

Claim 13 analyzed with respect to claim 1, Levitt further discloses a resistive element coupled between the filter network and the tuning circuit (Fig. 2 element 86, tri-state switch).

Claim 14 analyzed with respect to claim 13 and claim1, Levitt does not clearly disclose wherein a value of the resistive element is 500k ohms. However, it would be obvious to one of ordinarily skill in the art at the time the invention was made to set the value of the

resistive element to 500k ohms in the course of circuit design so as to limit current applied or as necessary.

Claim 15, Levitt discloses a hybrid circuit for buffering (Fig. 2) an audio signal comprising: a substrate having a first (Fig. 2) and second portion (Fig. 1), the second portion severable from the first portion (Fig. 1:124, EEPROM programming socket); and a buffer circuit substantially disposed on the first portion of the substrate, the buffer circuit comprising: a first input for coupling the audio signal (Fig. 2:element 57, microphone); a filter network coupled to the first input (Fig. 2, element 64); an output coupled to the filter network (Fig. 2, col. 5 line 7-11); a tuner for adjusting the filter network (Fig. 2:EEPROM); and a controller for altering a value of the tuner (Fig. 1 host controller), the controller having a second input, the second input disposed on the second portion of the substrate (Fig. 1 element 24, input from computer), whereby a tuning signal coupled to the second input is used to adjust the tuner (col. 4 line 38-43), thereby changing a transfer function of the buffer circuit (col. 4 line 30-33).

Claim 16, Levitt discloses wherein the controller retains a setting upon receiving the tuning signal (col. 4 line 38-43).

Claim 17 Levitt analyzed with respect to claim 15, Levitt discloses, wherein the second portion of the substrate (Fig. 1:124, EEPROM programming socket) and the controller

receives the tuning signal (col. 8 line 25-29). Levitt does not clearly disclose wherein the second portion of the substrate is permanently removed after the controller receives the tuning signal. However, it would be obvious to one ordinarily skilled in the art at the time the invention was made to permanently remove the programming device from the buffer circuit so that the circuit can perform the function it was programmed to without having an additional circuit attached.

Claim 19, Levitt discloses wherein the second input is further coupled to a biasing element, the biasing element maintaining a state after receiving the tuning signal (col. 5 line 34-37).

Claim 20 Levitt discloses, A method for adjusting a buffer circuit for use in a microphone assembly comprising:
providing a microphone housing and placing selected elements of the buffer circuit in the microphone housing (Fig. 2 col. 3 line 39-41and element 58 PROGR AGC) providing a desired response characteristic for the buffer circuit (col. 6 line 65-67); measuring an initial response characteristic of the buffer circuit (col. 6 line 68); comparing the desired response characteristic to the initial response characteristic (col. 7 line 1-2); determining an adjustment using the comparison, the adjustment for reducing a difference between the desired and initial response characteristics (col. 7 line 1-2); transmitting a signal to a selector circuit in the buffer circuit (col. 7 line 6-8);

and tuning an adjustable filter coupled to the selector circuit (col. 7 line 11-12), the adjustable filter for modifying the initial response characteristic (col. 7 line 65-67).

Levitt does not disclose a microphone housing and placing the buffer circuit in the microphone housing.
However Levitt discloses microphone housing and placing selected elements of the buffer circuit in the microphone housing (Fig. 2 col. 3 line 39-41and element 58 PROGR AGC).
Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made that the placement of selected elements within housing would be determined by space considerations and design choice.

Claim 22 analyzed with respect to claim 20, Levitt discloses transmitting the signal to the selector circuit (col. 8 line 25-29). Levitt does not clearly disclose removing a portion of the buffer circuit used in transmitting the signal to the selector circuit. However, it would be obvious to one ordinarily skilled in the art at the time the invention was made to permanently remove the programming device, (which has the portion for transmitting the signal to the selector circuit), from the buffer circuit so that the circuit can perform the function it was programmed to without having an additional circuit attached.

4. Claim 4-8, 18 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749) in view of Killion (5602925)

Claim 4 analyzed with respect to claim 1, Levitt does not disclose wherein the tuning circuit comprises a resistor network.

Killion discloses wherein the circuit comprises a resistor network (Figs. 6). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the resistor network of Killion in order to have at least one programmable resistor for setting the audio response of the hearing aid as taught by Killion (abstract line 1-3).

Claim 5 analyzed with respect to claim 1, Levitt does not disclose wherein the tuning circuit is a ladder network, the ladder network adjustable by activating a semiconductor device between an element of the ladder network and a ground connection. Killion discloses wherein the circuit is a ladder network (Fig. 6), the ladder network adjustable by activating a semiconductor device between an element of the ladder network and a ground connection (Fig. 6 col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the ladder network and semiconductor of Killion in order to save space when implementing the circuit and in order to have a silicon based switch that can be implemented with the rest of the circuit.

Claim 6 analyzed with respect to claim 5 and claim 1, Killion further discloses wherein the ladder network comprises one of resistors and capacitors (Fig 6).

Claim 7 analyzed with respect to claim 6, claim 5, and claim 1, Killion does not clearly disclose discloses wherein a resistor of the ladder network has a value of 5.5k ohms. However, it would be obvious to one of ordinarily skill in the art at the time the invention was made to set the value of the resistive element to 5.5k ohms in the course of circuit design so as to limit current applied or as necessary.

Claim 8 analyzed with respect to claim 5 and claim 1, Killion further discloses wherein the semiconductor device is a field effect transistor (FET) (Fig.6. col. 6 line 7-9).

Claim 18 analyzed with respect to claim 15, Levitt does not disclose wherein the tuner is a ladder network adjustable by activating a semiconductor device between an element of the ladder network and a ground network. Killion discloses wherein the tuner is a ladder network adjustable by activating a semiconductor device between an element of the ladder network and a ground network (Fig. 6. col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to implement the tuner of Levitt as a ladder network with a semiconductor in order to have a circuit that can be implemented on a chip.

Claim 23, Levitt discloses tuning the adjustable filter (col. 5 line 3-7) Levitt does not disclose, further comprises activating a semiconductor device between an element of a ladder network and a ground connection. Killion discloses activating a semiconductor device between an element of a ladder network and a ground connection (Fig. 6 col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the ladder network and semiconductor of Killion in order to save space when implementing the circuit and in order to have a silicon based switch that can be implemented with the rest of the circuit.

5. Claim 11, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable Levitt et al (4879749) in view of Advani et al. (4926459).
Claim 11 analyzed with respect to claim 1, 9, and 10. Levitt does not disclose wherein the biasing element is a zener-zap diode. Advani discloses wherein the biasing element is a zener-zap diode (Fig. 3; element 106, col.7 line 46-47). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with a zener-zap diode in order to utilize the breakdown characteristic of diodes.

Claim 24 analyzed with respect to claim 20, Levitt discloses tuning the adjustable filter (col. 5 line 3-7). Levitt does not disclose further comprises biasing the selector circuit with a zener-zap diode. Advani discloses further comprises biasing the circuit with a zener-zap diode (Fig. 3; element 106, col.7 line 46-47). Therefore it would be obvious to

one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with a zener-zap diode in order to utilize the breakdown characteristic of diodes.

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749) in view of Madaffari et al. (2002/0090102)

Claim 21 Levitt discloses a portion of the buffer circuit accessible from outside the housing (Fig. 1:element 24 col. 4 line 29). Levitt does not disclose assembling the buffer circuit in acoustically sealed housing. Madaffari discloses assembling the buffer circuit in acoustically sealed housing (Fig. 2 paragraph 15 line 13-15). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the housing of Madaffari in order to protect the circuit from EMI and other interferences.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FATIMAT O. OLANIRAN whose telephone number is (571)270-3437. The examiner can normally be reached on M-F 10:00-6 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FO
/Vivian Chin/
Supervisory Patent Examiner, Art Unit 2615